REMARKS

Claims 1-24 remain pending in this application. Claims 1, 7, 8, 15, 17 and 21 have been amended.

Rejection of Claim 1 under 35 USC § 102(b)

Claims 1-2, 9-14, 17, 18 and 20 are rejected under 35 USC § 102(b) as being anticipated by Badger (US Patent No. 5,678,211).

The present claimed invention recites a tuner. The tuner includes a phase-locked loop (PLL) circuit and a nonvolatile memory that stores alignment data. The alignment data is amplified by the phase-locked loop circuit. Limitations similar to those discussed above are found in all independent claims (Claims 1, 15, 17 and 21).

The claims have been amended to recite that the alignment data is processed by the phase-locked loop circuit. The amplification of the alignment data by the PLL allows for the creation of a television control system that exhibits modular tuner compatibility. The advantage of having modular tuner compatibility is the elimination of the need for microprocessor intervention for alignments which in turn increases the compatibility among the television receiver components. The benefits are described on page 2, line 3 to page 3, line 24. Support for the processing of alignment data by the PLL can be found on page 9, line 19- Page 10, line 28, and even more specifically on Page 10, line 11.

Badger discloses an arrangement including a microprocessor controller, PROM memory, and a digital to analog converter (DAC) arrangement for generating a plurality of control voltages for trimming respective ones of a plurality of varactor controlled tunable filters. The controller couples digital control signals to the respective DACs which generate respective analog control voltages which are applied to the respective tunable filters. A tuning voltage generated by a closed control loop, such as phased locked loop also under the control of the controller, is combined with the output

control voltages generated by the respective DACs in a resistance divider arrangement. Although the apparatus comprises a PROM, it is stated in column 2, lines 42-54 that the digital trimming control signals are received from the PROM via the microprocessor. Badger neither discloses nor suggests the "alignment data being processed by said phase-locked loop circuit" as in the present claimed invention. In Badger, by controlling the tuner adjustment data using the microprocessor, the compatibility among television receiver components is narrowed. The microprocessor must contain specific routines for selecting and communicating the alignment data from the nonvolatile memory to the tuner. The tuner must be adapted to accept the data and compensate for mismatches. As such, replacement of a malfunctioning television tuner in the field requires finding a new television tuner that is adapted to the specific television control system. The present claimed invention is provided to solve the deficiencies found in Badger, namely the control of tuner alignment data by the microprocessor, by using the Phase Lock Loop to control amplification of the alignment data.

In view of the above remarks and amendments to the claims, it is respectfully submitted that there is no 35 USC § 112 compliant disclosure in Badger showing the above discussed features. It is further respectfully submitted that claims 1, 15, 17 and 21 are not anticipated by Badger. As Claims 2, 3, 4, 5, and 9-14 are dependant on Claim 1, and Claims 18 and 20 are dependent on Claim 17, it is respectfully submitted that these claims are also allowable for the same reasons discussed above. It is thus respectfully submitted that these rejections are satisfied and should be withdrawn.

Rejection of Claims 6, 8, and 19 under 35 USC § 103(a)

Claims 6, 8 and 19 are rejected under 35 USC § 103(a) as being unpatentable over Badger (US Patent 5,678,211) in view of Bonneau et al. (US Patent 4,510,623).

Bonneau teaches an electronically tuned television receiver provided with a channel lockout feature to control viewer program selection. However, similarly to

Badger, Bonneau neither discloses nor suggests "alignment data being processed by said phase-locked loop circuit" as in the present claimed invention.

In view of the above remarks to the claims, it is respectfully submitted that Badger and Bonneau et al., when taken alone or in combination, provide no 35 USC § 112 compliant enabling disclosure showing the above discussed features. Thus, it is respectfully submitted that Badger and Bonneau et al., when taken alone or in combination, do not make the present invention as claimed in Claims 1 and 17 unpatentable. As Claims 6 and 8 are dependant on Claim 1, and Claim 19 is dependent on Claim 17, it is respectfully submitted that these claims are also allowable for the same reasons discussed above. It is thus respectfully submitted that these rejections are satisfied and should be withdrawn.

Rejection of Claim 7 under 35 USC § 103(a)

Claim 7 is rejected under 35 USC § 103(a) as being unpatentable over Badger (US Patent 5,678,211) in view of Bonneau et al. (US Patent 4,510,623) and in further view of Wu et al. (US Patent 6,557,117).

Wu et al. discloses an on-chip built-in self test apparatus for a phase-locked loop module that resides on an integrated circuit. Wu et al., however, neither discloses nor suggests "alignment data being processed by said phase-locked loop circuit" as in the present claimed invention.

In view of the above remarks to the claim, it is respectfully submitted that any combination of Badger, Bonneau et al. and Wu et al. provides no 35 USC § 112 compliant enabling disclosure showing the above discussed features. Thus, it is respectfully submitted that any combination of Badger, Bonneau et al. and Wu et al. does not make the present invention as claimed in Claim 1 unpatentable. As Claim 7 is dependant on Claim 1, it is respectfully submitted that Claim 7 is also allowable for the same reasons discussed above. It is thus respectfully submitted that these rejections are satisfied and should be withdrawn.

Rejection of Claims 15 and 16 under 35 USC § 103(a)

Claims 15 and 16 are rejected under 35 USC § 103(a) as being unpatentable over Badger (US Patent 5,678,211) in view of Mogi (US Patent 4,326,220).

Mogi discloses a television receiver that includes first and second signal receiving circuits. Mogi's invention, however, neither discloses nor suggests "alignment data being processed by said phase-locked loop circuit" as in the present claimed invention.

In view of the above remarks and amendments to the claims, it is respectfully submitted that Badger and Mogi, when taken alone or in combination, provide no 35 USC § 112 compliant enabling disclosure showing the above discussed features. Thus, it is respectfully submitted that Badger and Mogi, when taken alone or in combination, do not make the present invention as claimed in Claim 15 unpatentable. As Claim 16 is dependant on Claim 15, it is respectfully submitted that Claim 16 is also allowable for the same reasons discussed above. It is thus respectfully submitted that these rejections are satisfied and should be withdrawn.

Rejection of Claims 21, 22, and 24 under 35 USC § 103(a)

Claims 21, 22, and 24 are rejected under 35 USC § 103(a) as being unpatentable over Badger (US Patent 5,678,211) in view of Hisada et al. (US Patent 6,281,946).

Hisada teaches a television receiver having a tuner for converting a received signal from an antenna to an intermediate frequency signal, and supplying the intermediate frequency signal to a homodyne detector circuit. The Hisada invention also utilizes a demodulator to supply a demodulated video signal to a color cathode ray tube. Hisada, however, neither discloses nor suggests "alignment data being processed by said phase-locked loop circuit" as in the present claimed invention.

In view of the above remarks and amendments to the claims, it is respectfully submitted that Badger and Hisada, when taken alone or in combination, provide no 35 USC § 112 compliant enabling disclosure showing the above discussed features. Thus, it is respectfully submitted that Badger and Hisada, when taken alone or in combination, do not make the present invention as claimed in Claim 21 unpatentable. As Claims 22 and 24 are dependant on Claim 21, it is respectfully submitted that these claims are also allowable for the same reasons discussed above. It is thus respectfully submitted that these rejections are satisfied and should be withdrawn.

Rejection of Claim 23 under 35 USC § 103(a)

Claim 23 is rejected under 35 USC § 103(a) as being unpatentable over Badger (US Patent 5,678,211) in view of Hisada et al. (US Patent 6,281,946) in further view of Bonneau et al. (US Patent 4,510,623).

As mentioned previously, Bonneau teaches an electronically tuned television receiver provided with a channel lockout feature to control viewer program selection and Hisada teaches a television receiver having a tuner for converting a received signal from an antenna to an intermediate frequency signal, and supplying the intermediate frequency signal to a homodyne detector circuit. Bonneau's and Hisada's inventions neither disclose nor suggest "alignment data being processed by said phase-locked loop circuit" as in the present claimed invention.

In view of the above remarks to the claim, it is respectfully submitted that any combination of Badger, Hisada and Bonneau et al. provides no 35 USC § 112 compliant enabling disclosure showing the above discussed features. Thus, it is respectfully submitted that any combination of Badger, Hisada and Bonneau et al. does not make the present invention as claimed in Claim 21 unpatentable. As Claim 23 is dependant on Claim 21, it is respectfully submitted that Claim 23 is also allowable for the same reasons discussed above. It is thus respectfully submitted that these rejections are satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No additional fee is believed due. However, if an additional fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,
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September 30, 2004